Amendments to the Specification:

Replace paragraphs [0003], [0005], [0007], [0009], [0014]–[0015], [0025], [0029] and [0032] in their entireties with the paragraphs shown below.

[0003] For corresponding display parameters, a video graphics circuit calculates slopes and associated display parameters for each part within the triangle based on the slopes and corresponding display parameters. The slopes are associated with display parameters and are stored in a triangle descriptor list, which is subsequently used to calculate pixel information.

[0005] If only a small portion of an object is overlapped, the amount of unnecessary pixel information calculations are minimal, there is a minimal adverse affect on the video graphic circuit's efficiency. If, however, the object has a substantially overlapped portion, then the number of unnecessary calculations increases and the efficiency of the video graphics circuit is affected. This may be compounded where several objects have overlapping portions and only one object will be visible in the foreground and be entirely displayed. For example, assume that several faces are to be displayed and they overlap. To begin the display process, the video graphics circuit calculates the slopes and associated display ~~premise~~ parameters for each triangle of a face, which includes up to 20,000 triangles, and stores the value in the triangle descriptor list and stores the pixel information. The process is repeated for each face to be displayed. Once all of the pixel information is generated, the video graphics circuit compares the components of the faces to determine which one is in the foreground in the overlapped areas.

[0007] To overcome these inefficiencies, conventional video graphics circuits perform a hierarchical z-buffering technique. Hierarchical z-buffering is performed by comparing multiple pixels having the same x,y location, wherein the z value of a pixel is compared to a stored z value, where the stored z value represents the outermost visible pixel, i.e. having the highest z value. If the pixel to be rendered has a z value that is less than stored z value, the pixel is then

rendered because the pixel will be visible. Also, the z value is updated to represent the value of the rendered pixel, as any other pixels at the same location having a smaller z value will be hidden by the rendered pixel.

[0009] Although, conventional video graphics circuits cannot perform both hierarchical z-buffering and stencil operations because the circuit must choose to perform either the hierarchical z-buffering or the stenciling. The hierarchical Z buffering is typically disabled during the stencil test because the stencil test interacts with the Z buffering operation. Therefore, without a means of performing a hierarchical stencil test, it is in general impossible to know the correct result for a hierarchical depth test.

[0014] FIG. 3 is a schematic block diagram illustrating a video graphics processor ~~which is~~ in accordance with one embodiment of the present invention;

[0015] FIG. 4 is a schematic block diagram illustrating a video graphics processor ~~which is~~ in accordance with one embodiment of the present invention;

[0025] The first image 104 and the second image 106 also cast a first shadow 110 and a second shadow 112, respectively due to the position of the light source 102. The screen 100 displays images which not only overlap each other, but also produce non-visible portions. The first image 104 and the second image 106 block the visibility of the third image 108 because spatially, portions of the first image 104 and the second image 106 are displaced in front of third image 108. Also, the first shadow 110 and the second shadow 112 block the visibility of portions of the third image 108 as the shadows are also spatially disposed in front of the third image. ~~Also illustrated on the display 100 is that~~ As illustrated, on display 100, a portion of the first shadow 110 is not visible because a portion of the second image [[104]] 106 is spatially disposed in front of the first shadow 110.

[0029] The tile walker 136 provides the ~~tiles~~ tile's x,y address and the z plane 140 to a hierarchical Z and stencil logic 142. The hierarchical Z and stencil logic 142 retrieves a hierarchical Z value range and stencil codes from a hierarchical Z and stencil cache 144 in response to the tile x,y address and z plane, wherein the hierarchical Z value per tile is composed of a hierarchical cache MinZ, a hierarchical cache MaxZ and a stencil code. The hierarchical Z and stencil logic 142 thereupon performs a stencil test, as described below. If the stencil test reveals a likelihood that that at least one of the pixels in the tile is visible in light of the mask, the hierarchical Z and stencil logic 142 thereupon performs a hierarchical Z value test, as described below.

[0032] The tile walker 136 also provides the tile information to a buffer 148, which is operably coupled to the tile kill. When the tile kill receives the indicator, [[to]] the tile ~~information, the~~ information and the barycentric coordinates, are retrieved from the buffer 148 and either passed to a pixel walker 150 or killed by being discarded from the buffer.